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Abstract

Structural testing can lead to high and abnormal current surges.

Disclosed herein are methods for designing and testing an IC so that current surges therein may be minimized while the IC is being tested. One disclosed
5 way to minimize current surges is by gating out shift induced node state transitions. Another disclosed way to minimize current surges is to operate two or more of an IC's scan chains in parallel, but out-of-phase.